Agilent EEsof EDA

Low Noise Amplifiers using ATF-55143 Low Noise PHEMT

Agilent Technologies
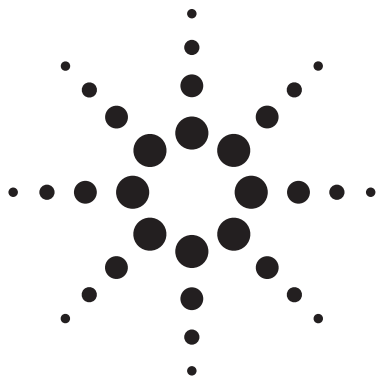
Low Noise Amplifiers for 5.125 - 5.325 GHz and 5.725 - 5.825 GHz Using the ATF-55143 Low Noise PHEMT

Application Note 1285

Description

This paper describes two low noise amplifiers for use in the IEEE 802.11a, ETSI/BRAN HiperLAN/2 5GHz standards. The circuits are designed for use with multi-layer 0.031 inch thickness FR-4 printed circuit board material. The 5.125-5.325 amplifier make use of low cost, miniature, multilayer chip inductors for small size. The 5.725-5.825 amplifier make use of printed inductors for small size and low cost. When biased at a V_{ds} of 2 volts and I_{ds} of 15 mA, the ATF-55143 amplifier will provide 10.0 to 11.0 dB gain, 1.2 dB noise figure and an output intercept point (IP3) of +24 to +27 dBm over the 5.1 - 5.8 GHz bandwidth. An active bias solution is discussed that uses a supply voltage of 3.3 volts and 5.0 volts. The design goals for both amplifiers are summarized in Table 1. The design is based on 0.813-mm (0.031 inch) thickness Grade FR4 copper laminate epoxy glass PC material, multi-layer board. The thickness between layers is 0.254-mm (0.010 inch). The amplifier schematic is shown in Figure 1, with component values in Table 2.

Introduction

The Agilent Technologies ATF-55143 is a low noise enhancement-mode PHEMT designed for use in low cost commercial applications in the VHF through 10 GHz frequency range. Agilent Technologies' new enhancement

Table 1. Design Goals

Parameter	Value
Gain	10.0 - 11.0 dB
Noise Figure, dB	< 1.5 dB
Output 3rd Order Intercept Point	> 25 dBm
Input 3rd Order Intercept Point	> 15 dBm
Output P-1dB Compression	> 10 dBm
Input return loss	> 10 dB
Output return loss	> 10 dB
Supply Current	15 mA

Figure 1. The Amplifier Schematic

Agilent Technologies
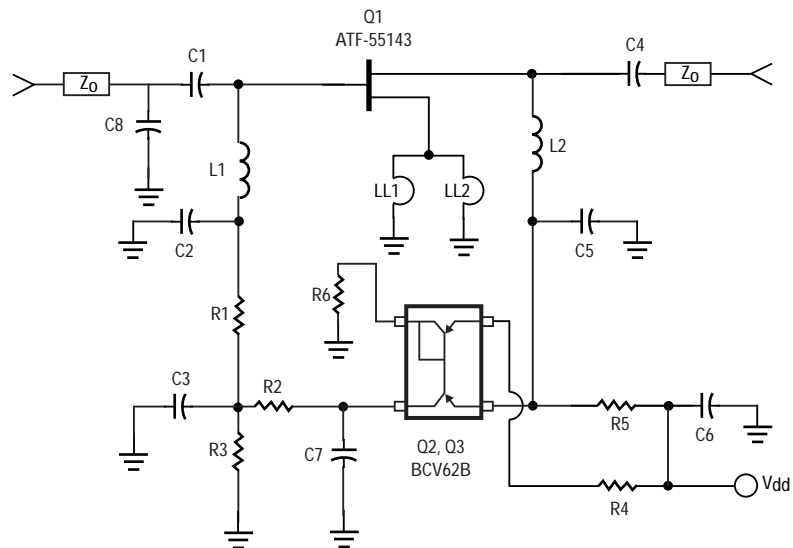
mode technology provides superior performance while allowing a dc grounded source amplifier with a single polarity power supply to be easily designed and built. Unlike a typical depletion mode PHEMT where the gate must be made negative with respect to the source for proper operation, an enhancement mode PHEMT requires that the gate be made more positive than the source for normal operation. Biasing an enhancement mode PHEMT is much like biasing the typical bipolar junction transistor. The ATF-55143 is a 400 micron gate width device with 2 GHz performance tested and guaranteed at a V_{ds} of 2.7 V and I_d of 10 mA. The ATF-55143 is housed in a 4-lead SC-70 (SOT-343) surface mount plastic package.

LNA Design

The two amplifiers were designed for V_{ds} of 2 volts and an I_{ds} of 15 mA. The amplifier schematic is shown in shown Figure 1. The 5.125-5.325 bandwidth amplifier uses a power supply voltage, V_{dd}, of 3.3 volt. The 5.725-5.825 bandwidth amplifier uses a power supply voltage, V_{dd}, of 5.0 volt. The generic demo board shown in Figure 2 is used. The demo board was designed such that the input and output impedance matching networks can be either lumped element networks or etched microstrip networks for lower cost. Either low pass or high pass structures can be generated based on system requirements. The demo board is etched on 0.031" thickness, multi-layer FR-4 material for cost considerations.

Biasing Options and Source Grounding

One of the advantages of the enhancement mode PHEMT is the ability to dc ground the source leads and still require only a

2

single positive polarity power supply. Whereas a depletion mode PHEMT pulls maximum drain current when $V_{gs} = 0$ V, an enhancement mode PHEMT pulls nearly zero drain current when $V_{gs} = 0$ V. The gate must be made positive with respect to the source for the enhancement mode PHEMT to begin pulling drain current. It is also important to note that if the gate terminal is left open circuited, the device will pull some amount of drain current due to leakage current creating a voltage differential between the gate and source terminals. Values for V_{gs} maybe calculated from the typical I-V curves found in the data sheet.

A voltage comparator bias option was chosen for the example as the same evaluation board is used for additional applications examples that require higher device voltage and source current while still running from a 3.3 volt supply voltage.

A suggested active biasing circuit is shown in Figure 1. The active biasing scheme uses the BCV62B current mirror bias circuit. The BCV62B has two PNP transistors in the same package; Q3 has the base and collector connected internally to the base of Q2. It behaves as a two-terminal pn diode, the voltage drop across the pn junction is typically 0.6 volts. The EB junction of Q3 is forward biased by exactly the same voltage as the EB junction of Q2. The two bipolars are operating like a voltage comparator, with the gate bias being adjusted to keep the voltages across R5 (and therefore I_d and V_{ds}) equal to the voltage across R4 which is determined by the potential divider R4, Q3Vbe and R6. Including the Q3Vbe junction in the potential divider chain temperature compensates Q2Vbe
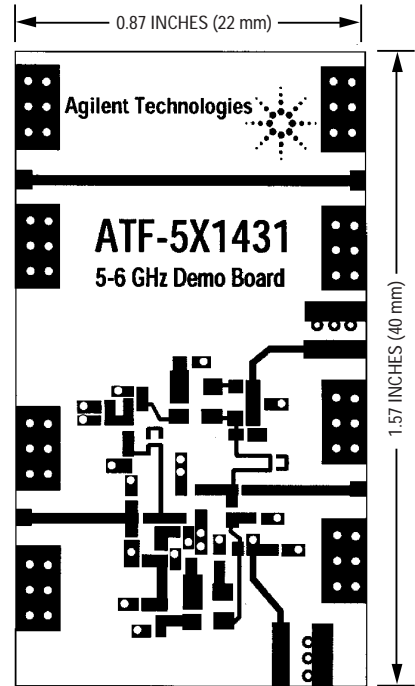

Figure 2. Artwork for the ATF-55143 Low Noise Amplifier

assuming the currents in the two PNP transistors are approximately equal. More details on active bias circuits may be found in references [4] and [6].

$$R6 \approx \frac{V_{DS} - Q2V_{be}}{I_{REF}}$$

$$R4 \approx \frac{V_{DD} - V_{DS}}{I_{REF}}$$

$$R5 \approx \frac{V_{DD} - V_{DS}}{I_{DS}}$$

Where:
I_{DS} is the desired drain current.
I_{REF} is the current flowing through the R6.
I_{REF} was chosen to be 1.4 mA.
$V_{DD} = 5$ V, $V_{DS} = 2$ V, $I_{DS} = 15$ mA,
$V_{gs} = 0.49$ V
$R6 = 1000 \ \Omega$
$R4 = 2200 \ \Omega$
$R5 = 200 \ \Omega$
$R2$ and $R3 = 1000 \ \Omega$

R2 and R3 act as a potential divider circuit with a ratio of 1:1, two 1 k ohm resistors were chosen. The collector voltage of Q2 should be 2 x V_{gs}.

An active bias circuit using a single PNP BJT is discussed in [2]. A passive circuit bias is discussed in [1].

The use of a controlled amount of source inductance can often be used to enhance LNA performance. Usually only a few tenths of a nanohenry or at most a few nanohenrys of inductance is required. This is effectively equivalent to increasing the source leads by only 0.032 inch or so. The effect can be easily modelled using Agilent Technologies *ADS*®. The usual side effect of excessive source inductance is very high frequency gain peaking and resultant oscillations. The larger gate width devices have less high frequency gain and therefore the high frequency performance is not as sensitive to source inductance as a smaller device would be.

Design of the ATF-55143 Amplifier

The parts list for the first amplifier is shown in Table 2. Inductors LL1 and LL2 are actually very short transmission lines between each source lead and ground. The inductors act as series feedback. The amount of series feedback has a dramatic effect on in-band and out-of-band gain, stability and input and output return loss. For the amplifier, each source lead is connected to its corresponding ground pad at a distance of approximately 0.032" from the source lead. The 0.032" is measured from the edge of the source lead to the closest edge of the first via hole.

Determining the Optimum Amount of Source Inductance

Adding additional source inductance has the positive effect of improving input return loss and low frequency stability. A potential down-side is reduced low frequency gain, however, decreased gain also correlates to higher input intercept point. The question then becomes how much source inductance can one add before one has gone too far? For an amplifier operating in the 900 MHz frequency range, excessive source inductance will manifest itself in the form of a gain peak in the 6 to 10 GHz frequency range. Normally the high frequency gain roll-off will be gradual and smooth. Adding source inductance begins to add bumps to the once smooth roll-off. The source inductance, while having a degenerative effect at low frequencies, is having a regen-

Table 2. Component Parts List for the ATF-55143 Amplifier

Frequency	5.125 - 5.325 GHz, 3.3 V Demo circuit	5.725 - 5.825 GHz, 5.0 V Demo circuit
C1	1.0 pF Johanson S402D chip capacitor	0.5 pF Johanson S402D chip capacitor
C2, C5	5.6 pF Johanson S402D chip capacitor	5.6 pF Johanson S402D chip capacitor
C3, C6, C7	10000 pF chip capacitor	10000 pF chip capacitor
C4	2.2 pF Johanson S402D chip capacitor	2.7 pF Johanson S402D chip capacitor
C8	0.3 pF Johanson S402D chip capacitor	Not Used
LL1, LL2	Source inductance of width 25 mil x length 32 mil microstrip between source and first via hole can be used to increase stability.	Source inductance of width 25 mil x length 32 mil microstrip between source and first via hole can be used to increase stability.
L1	3.9 nH Johanson L-07C3N9KT chip inductor	Printed 280 x 10 mil microstrip line
L2	1.0 nH Johanson L-07C1N0KT chip inductor	Shortened microstrip line to produce 100 x 10 mil using TCW
R1	47 Ω	47 Ω
R2, R3	1000 Ω	1000 Ω
R4	1100 Ω	2200 Ω
R5	82 Ω	180 Ω
R6	1100 Ω	1000 Ω
Q1	Agilent Technologies ATF-55143	Agilent Technologies ATF-55143
Q2, Q3	BCV62B, Philips or Infineon	BCV62B Philips or Infineon

erative effect at higher frequencies. This shows up as a gain peak in S21 and also shows up as input return loss S11 becoming more positive. Some shift in upper frequency performance is fine as long as the amount of source inductance is fixed and has some margin in the design so as to account for S21 variations in the device.

Figure 2 shows the artwork of the top RF layer of the ATF-5X143 evaluation board. The second layer is the groundplane and includes the dc connections required for the biasing network, the thickness between the top layer and second layer is 0.010". A third layer, which is also a groundplane, a further 0.010'' down and the 0.010" distance to the bottom of the board, makes up the additional material thickness and adds to the mechanical stability of the board, making the board a total of 0.031" thick. A 50 ohm line has been included on the board to aid the amplifier design. The 50 ohm line can also be used as a quick check that the board has been accurately manufactured. The 50 ohm line was found to have 0.5 dB insertion loss at 5.2 GHz, the return loss was measured at 23 dB. The Smith chart showed the board impedance was centered on 50 ohms. Capacitors and inductors being considered can be placed on the line to check to see if they are self-resonant in the amplifier bandwidth. This could be a potential problem.

Performance of the 5.125 - 5.325 GHz ATF-55143 Amplifier

The amplifier is biased at a V_{ds} of 2 volts and I_d of 15 mA. Typical V_{gs} is 0.49 volts. The board is modified as shown in Figure 3. The connection between the printed quarter-wave microstrip
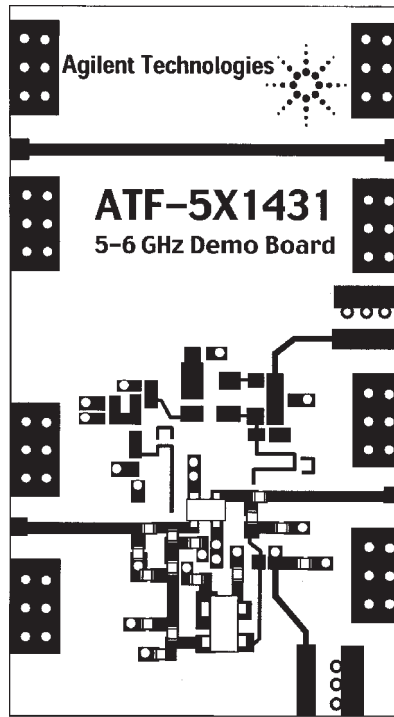

Figure 3. Component Placement Drawing for the 5.125-5.325 GHz ATF-55143 Low Noise Amplifier
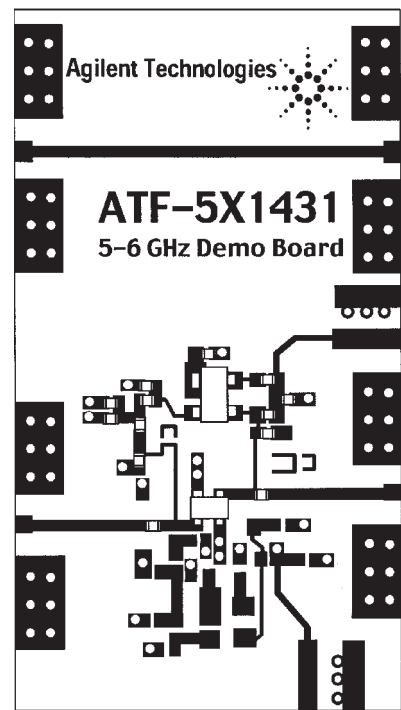

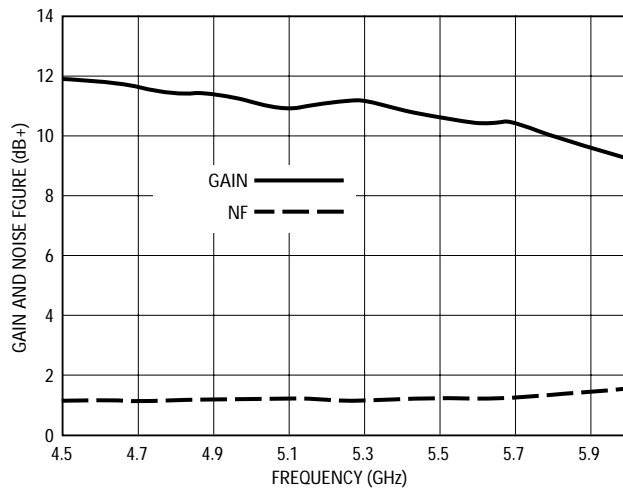Figure 4. Component Placement Drawing for the 5.725-5.825 GHz ATF-55143 Low Noise Amplifier

Figure 5. Gain and Noise Figure vs. Frequency

lines and RF track were removed. The measured noise figure and gain of the completed amplifier are shown in Figure 5. Noise figure is a nominal 1.2 dB from 5.0 through 5.4 GHz. A gain of 11.9 dB at 5.1 GHz and 11.7 dB at 5.3 GHz was measured.
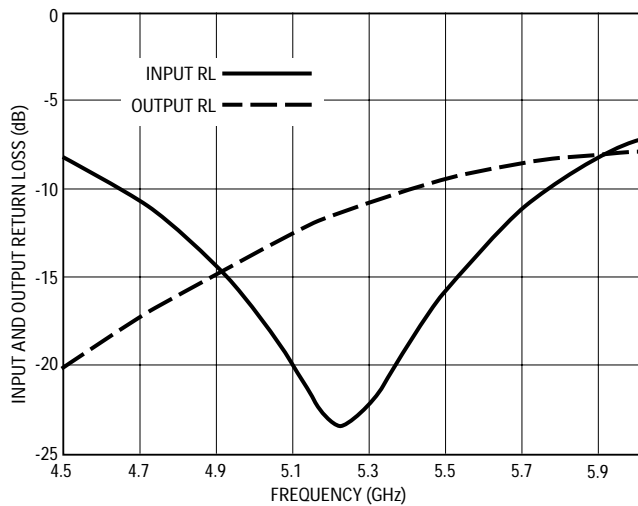
4

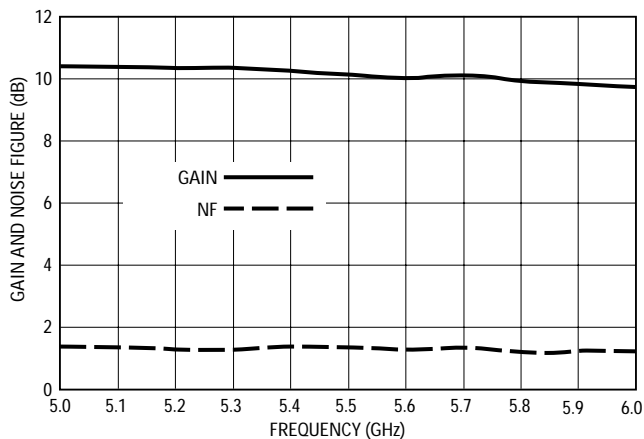**Figure 6. Input and Output Return Loss vs. Frequency**

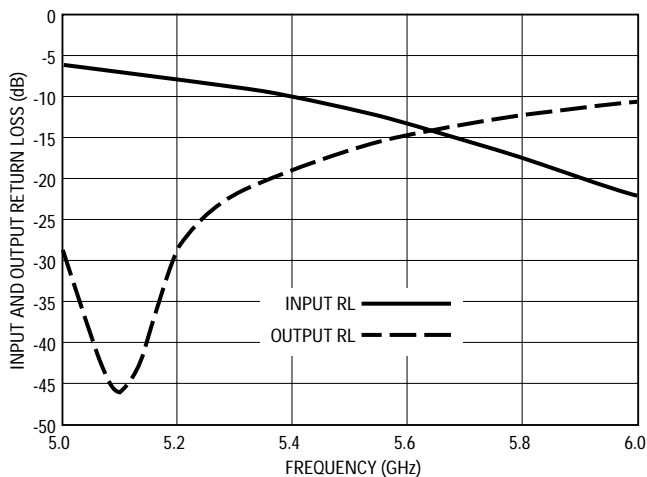**Figure 7. Gain and Noise figure vs. Frequency**

Figure 8. Input and Output Return Loss vs. Frequency

Measured input and output return loss is shown in Figure 6. The input return loss at 5.2 GHz is 23.3 dB with a corresponding output return loss of 11.5 dB. The amplifier output intercept point (OIP3) was measured at a nominal +26.5 dBm and P-1dB measured +10.5 dBm.

Performance of the 5.725 - 5.825 GHz ATF-55143 Amplifier
The amplifier is biased at a V_{ds} of 2 volts and I_d of 15 mA. Typical V_{gs} is 0.49 volts. The populated board using micro strip is shown in Figure 4. The measured noise figure and gain of the completed amplifier is shown in Figure 7. Noise figure is a nominal 1.3 dB from 5.5 through 6.0 GHz. Gain is a nominal 10.0 dB from 5.5 through 6.0 GHz.

Measured input and output return loss is shown in Figure 8. The input return loss at 5.8 GHz is 17.5 dB with a corresponding output return loss of 12.2 dB. The amplifier output intercept point (OIP3) was measured at a nominal +26 dBm and P-1dB measured +10.5 dBm.

ATF-55143 Low Noise Amplifier Design.
Using Agilent Technologies' Eesof Advanced Design System Software the amplifier's circuits can be simulated in both linear and non-linear modes of operation. The original design draft was a low noise amplifier with an Output Third Order Intercept Point (OIP3) of 25-27 dBm with a noise figure close to 1.2 dB at 5.125 - 5.325 GHz range and 1.4 dB in the 5.725 - 5.825 GHz range.

Linear Analysis
The ATF55143.s2p file can be downloaded from the Agilent Wireless Design Center web site. The 2-Port S-parameter file icon

5

available from the linear Data File Palette is used. A template for s-parameter evaluation is available in ADS, the Sparams_w Noise template was chosen. The circuit components were added to the simulation circuit. The more de-tailed the simulation the more accurate the results will be. An accurate circuit simulation can provide the appropriate first step to a successful amplifier design. The inductance associated with the chip capacitors and resistors was included in the simulation. Where possible models were cho-sen from the ADS SMT component library. Models of SMT components can also be obtained from the manufacturers' web sites. Manufacturing toler-ances in both the active and passive components often pro-hibit perfect correlation. The results of the simulated noise fig-ure, gain, input and output return losses are shown in Figures 9 and 10. The linear simulated perfor-mance of the amplifier was close to the measured results.

Return Loss vs. Frequency

As noted on the data sheet, the ATF-55143 S and Noise Param-eters are tested in a fixture that includes plated through holes through a 0.025" thickness printed circuit board. Due to the complex-ity of de-embedding these grounds, the S and Noise Param-eters include the effects of the test fixture grounds. Therefore, when simulating a 0.031" thick-ness, multi-layer, printed circuit board, only the difference in the printed circuit board thickness to the first ground layer has to be included. The distance to the first ground layer is only 0.010" in the simulation, i.e. 0.010" – 0.025" = – 0.015". Via holes with negative lengths are not allowable in ADS
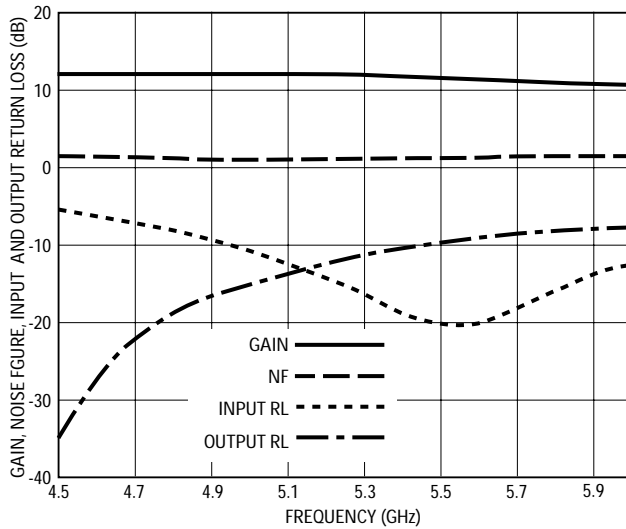

Figure 9. 5.125 - 5.325 GHz Amplifier Linear Simulated Gain, Noise Figure, Input and Output Return Loss vs. Frequency
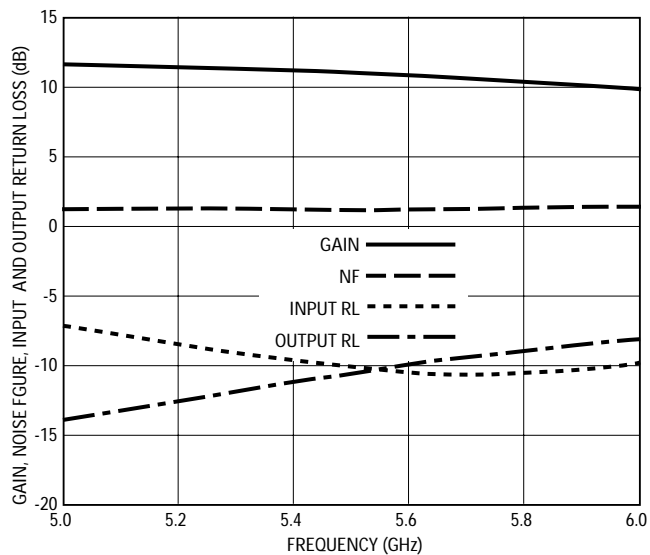

Figure 10. 5.725 - 5.825 GHz Amplifier Linear Simulated Gain, Noise Figure, Input and Output Return Loss vs. Frequency

simulation. The transmission lines that connect each source lead to its corresponding plated through hole is simulated as a microstripline (MLIN). The microstripline length can be used to include the effect of the im-proved grounding of the device.

Non-Linear Analysis

The circuit that is used for the non-linear analysis is identical to the linear analysis circuit. The 2-Port S parameter file icon was replaced by the non-linear model for the ATF-55143. The model was downloaded from the Agilent Wireless Design Center. The ADS unarchive function was used to extract the model. See ADS for further details on unarchiving models.

To perform the non-linear analysis the Harmonic Balanced controller or one of the other non-linear simulators must be inserted into the schematic window. The current probe and the node point were inserted to check that the bias conditions were correct.

The Non-Linear simulator allows us to simulate the P-1dB and the Output Third Order Intercept Point. The amplifier OIP3 was simulated at +22.3 dBm and P-1dB +10.25 dBm. Non-linear simulated performance of the amplifier was very close to the measured results for P-1dB but not for Output Third Order Intercept Point. A summary of the Non-linear simulated performance is shown in Table 3.

The non-linear transistor model used in the simulation is based on the work of Curtice [3]. An important feature of the non-linear model is the use of a quadratic expression for the drain current versus gate voltage. Although this model closely predicts the DC and small signal behavior (including noise), it does not predict the intercept point correctly. For example, the amplifier OIP3 was simulated at 22.3 dBm and the P-1dB at +10.3 dBm. The simulated performance for P-1dB was very close to the measured results, however, the simulated OIP3 was 2 - 3 dBm lower than the measured performance. To properly model the exceptionally high linearity of the E-PHEMT transistor, a better model is needed. This model, however, can still be used to predict the relative importance of output matching, bias, and source inductance.

Circuit Stability

Besides providing important information regarding gain, noise figure, input and output return loss, the computer simulation provides very important information regarding circuit stability. Unless a circuit is actually oscillating on the bench, it may be difficult to predict instabilities without actually presenting various VSWR loads at various phase angles to the amplifier. Calculating the Rollett Stability factor K and generating stability circles are two methods made considerably easier with computer simulations. The simulated gain, noise figure, and input/output return loss of the ATF-55143 amplifier is shown in Figures 9 and 10. These plots only address the performance near the actual desired operating frequency. It is still important to analyze out-of-band performance in regards to abnormal gain peaks, positive return loss and stability. A plot of Rollett Stability factor K as calculated from 0.1 GHz to 12 GHz is shown in Figure 11 for the amplifier. Source inductance can be used to help stability. It should be noted however that excessive inductance will cause high frequency stability to get worse (i.e. decreased value of K). As stability is improved, certain amplifier parameters such as gain and power output may have to be sacrificed.

Conclusion

The amplifier design has been presented using the Agilent Technologies ATF-55143 low noise PHEMT. The ATF-55143 provides a very low noise figure along with high intercept point making it ideal for applications where high dynamic range is required. In addition to providing low noise figure, the ATF-55143 can be simultaneously matched for very good input and output return loss, making it easily cascadable with other amplifiers and filters with minimal effect on system passband gain ripple.

Table 3

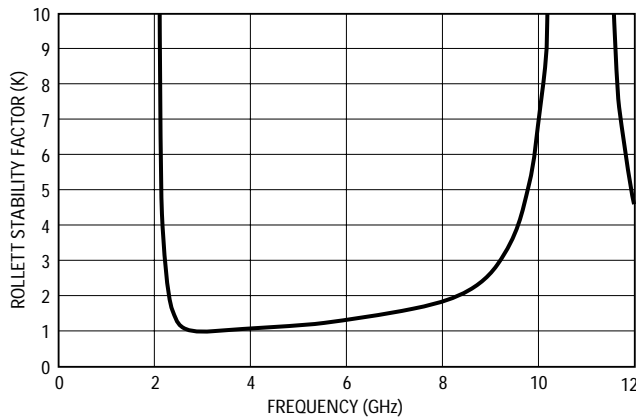| Frequency, Bias Conditions	P-1dB	Third Order Intercept
5.25 GHz, 2 V, 15 mA	10.7 dBm	23.5 dBm
5.73 GHz, 2 V, 15 mA	10.3 dBm	22.3 dBm

Figure 11. Simulated Rollett Stability Factor K

References

Performance data for ATF-55143 PHEMT may be found on http://www.agilent.com/view/rf

Agilent Application Notes:

[1] Agilent Application Note 1241: "A Low Noise High Intercept Point Amplifier for 1930 to 1990 MHz using the ATF-55143 PHEMT ", A.J. Ward.

[2] Application Note 1222: "High Intercept Low Noise Amplifier for the 1850 – 1910 MHz PCS Band using the Agilent ATF-54143 Enhancement Mode PHEMT ", A.J. Ward.

[3] W. R. Curtice, "A MESFET model for use in the design of GaAs integrated circuits," *IEEE Trans Microwave Theory Tech*, vol. MTT-28, pp. 448-456, May 1980.

[4] Dragan Maksimovic: 3 Operating modes: the key to finding DC bias solution, *ECEN4228 Course Notes.*

[5] Application Note: "High Intercept Low Noise Amplifier for 2.4 GHz ISM Applications using the ATF-551M4 Enhancement Mode PHEMT ", A.J. Ward.

[6] The Art of Electronics – Paul Horowitz and Winfield Hill – Cambridge ISBN 0521370957.

Agilent Technologies

For more information about
Agilent EEsof EDA, visit:

www.agilent.com/find/eesof

www.agilent.com

For more information on Agilent Technologies'
products, applications or services, please
contact your local Agilent office. The
complete list is available at:

www.agilent.com/find/contactus

Americas

Canada	(877) 894-4414
Latin America	305 269 7500
United States	(800) 829-4444

Asia Pacific

Australia	1 800 629 485
China	800 810 0189
Hong Kong	800 938 693
India	1 800 112 929
Japan	0120 (421) 345
Korea	080 769 0800
Malaysia	1 800 888 848
Singapore	1 800 375 8100
Taiwan	0800 047 866
Thailand	1 800 226 008

Europe & Middle East

Austria	0820 87 44 11
Belgium	32 (0) 2 404 93 40
Denmark	45 70 13 15 15
Finland	358 (0) 10 855 2100
France	0825 010 700*
	*0.125 €/minute
Germany	01805 24 6333**
	**0.14 €/minute
Ireland	1890 924 204
Israel	972-3-9288-504/544
Italy	39 02 92 60 8484
Netherlands	31 (0) 20 547 2111
Spain	34 (91) 631 3300
Sweden	0200-88 22 55
Switzerland	0800 80 53 53
United Kingdom	44 (0) 118 9276201

Other European Countries:
www.agilent.com/find/contactus
Revised: March 27, 2008

Product specifications and descriptions
in this document subject to change
without notice.

✳ **Agilent Technologies**

射 频 和 天 线 设 计 培 训 课 程 推 荐

易迪拓培训(www.edatop.com)由数名来自于研发第一线的资深工程师发起成立，致力并专注于微波、射频、天线设计研发人才的培养；我们于 2006 年整合合并微波 EDA 网(www.mweda.com)，现已发展成为国内最大的微波射频和天线设计人才培养基地，成功推出多套微波射频以及天线设计经典培训课程和 ADS、HFSS 等专业软件使用培训课程，广受客户好评；并先后与人民邮电出版社、电子工业出版社合作出版了多本专业图书，帮助数万名工程师提升了专业技术能力。客户遍布中兴通讯、研通高频、埃威航电、国人通信等多家国内知名公司，以及台湾工业技术研究院、永业科技、全一电子等多家台湾地区企业。

易迪拓培训课程列表：http://www.edatop.com/peixun/rfe/129.html

射频工程师养成培训课程套装

该套装精选了射频专业基础培训课程、射频仿真设计培训课程和射频电路测量培训课程三个类别共 30 门视频培训课程和 3 本图书教材；旨在引领学员全面学习一个射频工程师需要熟悉、理解和掌握的专业知识和研发设计能力。通过套装的学习，能够让学员完全达到和胜任一个合格的射频工程师的要求…

课程网址：http://www.edatop.com/peixun/rfe/110.html

ADS 学习培训课程套装

该套装是迄今国内最全面、最权威的 ADS 培训教程，共包含 10 门 ADS 学习培训课程。课程是由具有多年 ADS 使用经验的微波射频与通信系统设计领域资深专家讲解，并多结合设计实例，由浅入深、详细而又全面地讲解了 ADS 在微波射频电路设计、通信系统设计和电磁仿真设计方面的内容。能让您在最短的时间内学会使用 ADS，迅速提升个人技术能力，把 ADS 真正应用到实际研发工作中去，成为 ADS 设计专家…

课程网址：   http://www.edatop.com/peixun/ads/13.html

HFSS 学习培训课程套装

该套课程套装包含了本站全部 HFSS 培训课程，是迄今国内最全面、最专业的 HFSS 培训教程套装，可以帮助您从零开始，全面深入学习 HFSS 的各项功能和在多个方面的工程应用。购买套装，更可超值赠送 3 个月免费学习答疑，随时解答您学习过程中遇到的棘手问题，让您的 HFSS 学习更加轻松顺畅…

课程网址：http://www.edatop.com/peixun/hfss/11.html